REMARKS

(A) 35 USC 112 Rejection: (Claim 10)

In section 2 of the office action, the examiner noted that Claim 10 is rejected under 35 USC 112, second paragraph, as being indefinite for failing to point out and distinctly claim the subject matter which applicant regards as the invention. The amended Claim 10 distinctly identifies and claims the subject matter. Withdrawal of the rejection is respectfully requested.

(B) 35 USC 102(a) Rejection: (Claims 1-22)

In section 4 of the office action, the examiner noted that Claims 1-22 are rejected under 35 USC 102(a) as being anticipated by Sugibayashi et al. (US 6,515,511).

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. "Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."

The applicant discloses techniques to construct configuration circuits comprising (either memory circuits or hard-wire circuits) vertically above logic gates for programmable circuits that are convertible to application specific circuits. Furthermore, the applicant identifies a method to replace memory circuits (memory element and pass-gate) with hard-wires to facilitate the conversion. In contrast, Sugibayashi discloses a technique to construct only transfer gates above logic gates. He does not identify a technique to construct memory elements above the logic layer and he does not identify a method to replace memory circuits and transfer-gate circuits with hard-wire circuits.

Independent Claim-1 rejection: With respect to Applicant's claim 1, in the Office Action, section 5, the examiner noted that:

> "With respect to claim 1, figures 3-24 of Sugi discloses a programmable wire structure for an integrated circuit, comprising: ...; and a configuration circuit (wiring circuit 38 carrying signal to control transistor) coupled to said programmable switch, said circuit comprising a means to program said switch between said first and second state; and ..."

In Figs. 3-24 wiring circuits 38 (has no memory element) does not comprise a configuration circuit as defined by the Applicant. On Application page 21, line 6, the Applicant defines configuration circuit to include the memory element as follows:

> "The term configuration circuit includes one or more configurable elements and connections that can be programmed for controlling one or more circuit blocks in accordance with a predetermined user-desired functionality. The configuration circuit includes the memory element and the access circuitry, herewith called memory circuitry, to modify said memory element. Configuration circuit does not include the logic pass-gate controlled by said memory element. In one embodiment, the configuration circuit includes a plurality of memory circuits to store instructions to configure an FPGA. In another embodiment, the configuration circuit includes a first selectable configuration where a plurality of memory circuits is formed to store instructions to control one or more circuit blocks. The configuration circuits include a second selectable configuration with a predetermined conductive pattern formed in lieu of the memory circuit to control substantially the same circuit blocks. The memory circuit includes elements such as diode, transistor, resistor, capacitor, metal link, among others. The memory circuit also includes thin film elements. In yet another embodiment, the configuration circuits include a predetermined conductive pattern, via, resistor, capacitor or other suitable circuits formed in lieu of the memory circuit to control substantially the same circuit blocks".

Sugibayashi combines a wire connection portion comprising thin film transistors over a logic gate portion comprising MOS transistors. The thin film transistor serves as a transfer gate to couple wires. Configuration circuit comprising SRAM memory is constructed in the logic gate portion. The data in SRAM configures the thin film transfer gates. This is stated by Sugi as follows. First, in para 1, line 38, it is stated that memory cells control the ON/OFF characteristics of the transfer gate. Second, in para 5, line 23 it is stated:

> "As illustrated in Fig-4, the basic cell is composed of a logic gate portion 4 and a wire selection portion 7. The logic gate portion 4 includes a programmable logic gate 6, and an SRAM 5 for programming the programmable logic gate."

Third, in para 5, line 33 it is stated:

> "An ON/OFF operation of each switch 8,9 in the wire selection portion 7 is controlled by a data signal stored in the SRAM 5. Herein the data signal can be written into the SRAM 5 by the use of a ROM, an EPROM and an EEPROM when a power supply is introduced".

In Sugibayashi teaching, there is no disclosure of a configuration circuit, constructed either as SRAM memory or any other form of memory, above a metal layer. As the logic gate portion includes the SRAM memory, one or more of Figs. 7, 8, 9, 11, 12, 14, 16 & 17 can be

used to identify the location of this SRAM. In all of these Figures, layer 30 is the location of the first metal (the lowest metal layer in the stack), while layers 24 & 25 are the gates of MOS transistors. With reference to Fig. 7, the gate layer is identified in para 6, line 38-46, and the lowest metal layer is identified in para 6, line 48. While the SRAM cell construction is not detailed by Sugi, it is well known from prior art that an SRAM cell comprises MOS transistors, such as those shown by Sugi in Fig. 7 with gates 24 & gate 25. Clearly these gates 24 & 25 are located below the metal layer 30 by the thickness of the dielectric 28, which is further emphasized in para 6, line 47 as:

> "Further, an interlayer insulating film 28 is placed on the substrate. A first layer, a second layer, and a third layer wiring patterns 30, 32, 38 are formed in the interlayer insulating film."

Claim 1 in the current application claims:

> 1. (As Filed) A programmable wire structure for an integrated circuit, comprising:
> a programmable switch coupling two nodes, said switch having a first state that connects said two nodes, and said switch having a second state that disconnects said two nodes; and
> a configuration circuit coupled to said programmable switch, said circuit comprising a means to program said switch between said first and second state; and
> a first metal layer fabricated above a silicon substrate layer, said switch and said configuration circuit fabricated substantially above said first metal layer.

Sugibayashi fails to demonstrate: a first metal layer fabricated above a silicon substrate layer, said switch and said configuration circuit fabricated substantially above said first metal layer. Specifically, Sugibayashi fails to expressly or inherently demonstrate both configuration circuit (comprising the SRAM memory element 5 in Fig-4) and the thin film transfer gate (8 in Fig-4) fabricated substantially above a first metal layer (30 in Fig-7). This is further illustrated below.

In Sugi Fig-14A, the wiring circuit 38 couples to the gate 35 of the transfer device. Sugi does not show or describe how the transfer gate node 35 is coupled to the SRAM memory element in Fig-14, but it can be inferred from Fig-5. In Fig-5, the SRAM cell 5a is shown coupled to TFT device Qe as described in para 5, line 51. The wire 38 shown in Fig-14A would be a small portion of the wire connection extending from the SRAM cell 5a to the TFT gate Qe. The configuration circuit (according to the Applicant's definition, and duplicated herein) comprises the memory element 5a, and the decoding circuitry required to configure cell 5a

(which is hidden inside the block marked as SRAM cell 5a). In para 8, line 30, Sugi specifically states that the SRAM (and logic) portion in Fig-14 is identical to that in Fig-7.

Furthermore, Sugi fails to identify the motivation for the configuration circuit to be fabricated above the first metal layer, within the transfer-gate module. His identified values for only transfer gates to be fabricated above logic gates are described in para 2, lines 4-25. In summary, the listed advantages are: (a) reduction from TFT junction capacitance, (b) reduction in vertical wire lengths hence capacitance due to the position of TFT transfer gates, (c) reduction of wire resistance from shorter vertical wire height due to (b), and (d) increased gate density from stacking TFT transfer gates over logic. The TFT transfer gate ON resistance is significantly larger than an equivalent MOS transfer gate, and any advantage in (a) – (c) listed above will be totally negated due to the higher $(R_{ON})*(C_{WIRE}+C_{JUNC})$ component. Thus the only realistic advantage is in the reduction in Si area due to the TFT transfer gate vertical construction.

In contrast, the Applicant describes some of the advantages in constructing configuration circuits and pass-gates with TFT transistors, in page 13, line 22 as:

> "Configuration circuits, including configuration memory, constructed on same silicon substrate take up a large Silicon foot print. That adds to the cost of programmable wire structure compared to a similar functionality custom wire structure. A 3-dimensional integration of pass-gate and configuration circuits to connect wires provides a significant cost reduction".

More on page 15, line 10 as:

> "A programmable wire structure has the customization circuitry confined to a TFT layer above the fixed structured cell layer. This TFT module may be inserted to a logic process. Manufacturing cost of TFT layers add extra cost to the finished product. Once the programming is finalized by the user, the final interconnect pattern is fixed for most designs during product life cycle. Programmable wire circuits are no longer needed. The user can convert the design to a lower cost hard-wire custom device with an identical interconnect pattern. The programmed connection is mapped to a metal connection in the hard-wire option. This may be done with a single metal mask in lieu of all of TFT layers in the second module. The first module with structured cells does not change by this conversion".

And furthermore on page 17, line 9 as:

> "The programmable interconnect structure constitutes fabricating a VLSI IC product. The IC product is re-programmable in its initial stage with turnkey conversion to a one mask customized ASIC. The IC has the end ASIC cost structure and initial FPGA re-programmability. The IC product offering occurs in two phases: the first phase is a

generic FPGA that has re-programmability contained in a programmable wire structure, and a second phase is an ASIC that has the entire programmable module replaced by one or two customized hard-wire masks. Both FPGA version and turnkey custom ASIC has the same base die. The vertically integrated programmable module does not consume valuable silicon real estate of a base die. Furthermore, the design and layout of these product families adhere to removable module concept: ensuring the functionality and timing of the product in its FPGA and ASIC canonicals".

One with ordinary skill would not have the rationale to modify the Sugibayashi invention to construct memory circuits and transfer gates in the thin film layers as presented by the Applicant. The disadvantages of TFT described by Sugi on para 3, line 27 would prevent a reader endorsing the use of TFT layers for memory construction due to the "delay operation, large leak and low heat-dissipation characteristic". Therefore vertically integrated memory construction is not expressly or impliedly stated in the listed prior art, and a *prima facie* case of obviousness has not been met; it would not be obvious to one with ordinary skill to arrive at the Applicants disclosure stated in the independent Claim 1. Applicant's Claim-1 would have not been obvious under Sugibayashi. Withdrawal of the rejection of Claim-1, and those dependent thereupon (Claims 2-10) is respectfully requested.

Dependent Claim-6 rejection: With respect to Applicant's claim 6, in the Office Action, section 10, the examiner noted that:

> "With respect to claim 6, figures 14A of Sugi discloses at least one of said first (39) and second (28) nodes of said programmable switch further comprised a via structure (39), said via structure containing a seed metal, said seed metal facilitating a thermally activated phase change of at least one of said thin film materials to improve conduction of said connect state (metal connection as shown in figure 14A improves conduction)."

In Figs. 14A, Sugibayashi does not show either seed metal inside via plugs, or seed metal induced phase change of poly-silicon thin film materials. In Fig-14A, the poly-silicon thin film materials are labeled 34, 35 & 36. Source and drain regions are denoted 36, while the channel region is denoted 35. The fifth conductive plug 39 contacts the thin film the source/drain region 36 (para 8, line 36 & para 10, line 1). In Sugi, there is no disclosure of any enhancements to via plugs (such as 39) formations, nor any disclosure of how a seed material in plug 39 can enhance the transfer-gate ON conductivity. In para 12, line 54 Sugi discusses how poly silicon thin-film mobility can be enhanced by irradiating a laser beam.

In contrast, in Figs. 7.8A/B and 7.9A/B, the Applicant discusses how seed material can be incorporated into the via plug structure such that the poly-silicon thin film mobility can be enhanced by MILC (metal induced laser crystallization). This is further described by the Applicant on page 36, line 16 as follows:

> "The Via-2 plug formation is modified from typical processing techniques to include Ni metal to help reduce poly crystallization temperature. In other embodiments, the Via-2 plug may have a different seed metal to assist MILC, or have no seed metal at all. Lowering temperature makes the TFT module compatible with Aluminum and Copper metallization schemes used in sub 0.18 micron technologies. In a first embodiment shown in Fig-7.8A, Via-2 is filled with Ti 701, TiN 702 for the glue layer followed by W 703 and Ni 704 deposition to fill the plugs. The W 703 thickness is chosen to cover most of the via-hole with W and for Ni 704 to fill just the center. Wafer surface is then CMP polished as shown in Fig-7.8B to leave the fill materials only in the Via-2 holes. After the polish, Ni is located only at the very center of Via-2 holes. In a second embodiment shown in Fig-7.9A, Via-2 is filled with Ti 711, TiN 712 for the glue layer followed by Ni 714 and W 713 deposition to fill the plugs. The Ni 714 thickness is chosen to thinly cover Ti/TiN glue layer, and for W 713 to completely fill the via-hole. Wafer surface is then CMP polished as shown in Fig-7.9B to leave the fill materials only in the Via-2 holes. After the polish, Ni is located as a thin ring adjacent to Ti/TiN glue layer inside the Via-2 holes. These methods and others easily adapted by one skilled in the art provides Ni nucleation sites inside the via-holes to grow single crystal grains from deposited poly silicon during a later MILC step. The thickness of Ni is controlled to form Nickel-Salicide only near the proximity of the via-hole."

Plug 39 in Sugibayashi simply assists in contacting the source/drain region of the poly-silicon thin-film transfer gate. The plug makes no impact on the thin film materials to improve conduction as stated by the applicant. Withdrawal of the rejection is respectfully requested.

Independent Claim-11 rejection: With respect to Applicant's claim 11, in the Office Action, section 14, the examiner noted that:

> "With respect to claim 11 & 15, figures 14A of Sugi discloses a wire structure for an integrated circuit having two selectable methods of connecting wires, comprising:
> a first selectable method comprising programmable switches (34-35), each said switch coupling a wire in a first set (to a wire in a second set, and said method providing a means to program a user defined interconnect pattern between said first and second set of wires;
> and a second selectable method comprising permanent connections in lieu of said switches, said permanent connection pattern duplicating one of said user defined interconnect patterns (vias connection from 30 to 32)"

The Applicant has appended Claim-11 to better present the new invented matter. Appended Claim 11 in the current application now claims:

> 11. (Currently Amended) A wire structure for an integrated circuit having two selectable methods of connecting wires, comprising:
> a first selectable method comprising programmable switches, each said switch coupling a wire in a first set to a wire in a second set, and said method providing a means to program a user defined interconnect pattern between said first and second set of wires; and
> a second selectable method comprising permanent connections ~~in lieu of said switches~~, each switch in said first selectable method replaced by a connected or a disconnected wire, said permanent connection pattern duplicating one of said user defined interconnect patterns.

Sugibayashi fails to demonstrate: a second selectable method comprising permanent connections, each switch in said first selectable method replaced by a connected or a disconnected wire.

Sugibayashi in Fig-14A does not show a second selectable method of connecting wires wherein the programmable switch of the first selectable method is replaced by a connected or disconnected wire. For example, in figure 14A, two programmable switches are shown: the left switch and the right switch. Wire 32 connects to 34 through the right switch, and to an unlabeled wire through the left switch. Wire 32 is in the first set of wires, and wire 34 & unlabeled wire are in the second set of wires. A first selectable method of connecting wires is shown in Fig-14A, wherein each programmable switch (transfer device) connects wire 32 to either 34 or unlabeled wire. In this first selectable method, in addition to programmable switches, there are fixed connections as well. Wire 32 connects to wire 30 through such a permanent via. Wire 30 does not belong either to first set or the second set. The user is only allowed to program the wire connections coupled by the programmable switches, and not those that are hard-wired. The user defines an interconnect pattern by programming the SRAM memory content to hold data to turn the switches ON or OFF. One such pattern may be achieved with ON state right switch and an OFF state left switch. The Applicant has introduced new invented matter wherein the ON and OFF state of the switches can be replaced by hard-wire connections, eliminating the switches completely. Such a second selectable method is not available in Sugibayashi teaching.

The Applicant illustrates the two methods of connecting wires in the pairs of figures (7.6 & 7.7), (8A & 8B/8C), (9A, 9B/9C), (10C & 10D) in Application 10/727,170. In the first

selectable method, the programmable structures 7.6, 8A, 9A & 10C are fabricated with configuration memory elements. In the second selectable method the hard wired structure 7.7, 8B/8C, 9B/9C & 10D are fabricated without the memory element. In the second option, the programmable switch is completely eliminated from the fabrication method.

Furthermore, Sugi fails to identify the motivation for replacing programmable configuration circuits in the first option with hard-wire configuration circuits in the second option. There is no mention of configuration circuits in the document. The Applicant has stated the advantage of such a scheme on page 10, line 22 as follows:

> "What is desirable is to have programmable version to a structured ASIC device at the beginning of a design cycle. The user can program such an off-the-shelf device, place logic and routing at an optimal location to improve timing or cost of said design. The flexibility is further enhanced when the logic element contains programmable elements such as LUTs. For an emulation device, the cost of programmability is not a concern if such a device lends to easy design porting to a hard-wire low cost version once the design is finalized. Such a conversion has to keep the timing of the original design intact to avoid valuable re-engineering time and cost. Such a conversion should lower the end product cost to be competitive with an equivalent standard cell ASIC cost for design opportunities that forecast fairly significant volumes. These programmable structured ASIC devices will target applications that are cost sensitive, have short life cycles and demand volumes larger than for typical FPGA designs and lower than for typical ASIC designs."

One with ordinary skill would not have the rationale to modify the Sugibayashi invention to construct memory circuits in the thin film layers such that they could be replaced by hard-wires. Due to the disadvantages of TFT described by Sugi on para 3, line 27 would prevent a reader endorsing the use of TFT layers for memory construction due to the "delay operation, large leak and low heat-dissipation characteristic". Therefore vertically integrated memory construction & replacement of such memory with hard-wires is not expressly or impliedly stated in the prior art. Hence a *prima facie* case of obviousness has not been met; it would not be obvious to one with ordinary skill to arrive at the Applicants disclosure stated in the independent claim 11. Hence Applicants Claim-11 would have not been obvious under Sugibayashi. Withdrawal of the rejection of Claim-11, and those dependent thereupon (Claims 12-17) is respectfully requested.

Independent Claim-18 rejection: With respect to Applicant's claim 18, in the Office Action, section 16, the examiner noted that:

> "With respect to claim 18, the apparatus of Sugi discloses a semiconductor device for integrated circuits with two selectable manufacturing configurations, comprising:
> a first module layer having an array of structured cells (bottom layer, figure 14A), said module layer having one layer of metal (30);
> and a second module layer formed substantially above said first module layer comprising two selectable configurations, wherein: in a first selectable configuration a programmable interconnect structure (transistors include elements 34-36) is formed to connect said structured cells, and in a second selectable configuration a customized interconnect structure (vias between 32 and 30) is formed to connect said structured cells"

Claim 18 in the current application claims:

> 18. (As Filed) A semiconductor device for integrated circuits with two selectable manufacturing configurations, comprising:
> a first module layer having an array of structured cells, said module layer having at least one layer of metal; and
> a second module layer formed substantially above said first module layer comprising two selectable configurations, wherein:
> in a first selectable configuration a programmable interconnect structure is formed to connect said structured cells, and
> in a second selectable configuration a customized interconnect structure is formed to connect said structured cells.

Sugibayashi fails to demonstrate: a second module layer formed substantially above said first module layer comprising two selectable manufacturing configurations, wherein: in a second selectable configuration a customized interconnect structure is formed to connect said structured cells. Fig-14A does not show two selectable manufacturing configurations for the second module layer comprising programmable and a customized interconnect structure. Sugi shows only one manufacturing configuration to connect the structured cells in the first module layer of Fig-14A comprising both programmable elements (transistors include elements 34-36) AND customized elements (vias between 32 and 30). For example, in figure 14A, the connection between wire 34 and 32 has only the programmable connection, the transistor with elements 34-36, controlled by an SRAM cell. The transistor may be programmed to be ON or OFF by the data content in the SRAM cell. There is no second manufacturing configuration for connecting wire 32 to 34 without the thin film transfer-gate, or without the SRAM cell. Similarly the connection between wire 32 and 30 also has only one customized connection, the via between 32 and 30. This is

always connected and there is no second manufacturing configuration. Both the programmable portion and customized portion must coexist in the only available manufacturing configuration to render the device in Fig-14A functional. Hence, the second module layer in Fig-14A has only one manufacturing configuration comprised of the via connecting wire 32 to 30, and the transfer-gate connecting wire 32 to 34.

The Applicant defines a module layer on page 20, line 18 of the application as:

> "The term module layer includes a structure that is fabricated using a series of predetermined process steps. The boundary of the structure is defined by a first step, one or more intermediate steps, and a final step. The resulting structure is formed on a substrate."

The second module layer in Fig-14A may be identified by the first, the intermediate steps and the final step per Applicant's definition. The examiner has identified the via between wires 30 & 32, and the transistor between wires 32 & 34 to be in the second module. The first step in this second module layer from Fig-14A is the lower insulation layer 28 deposition (above metal 30) and the last step is wire 34 formation. The intermediate steps of the second module layer includes plug formation between metal 32 & 30, wire 32 formation, thin-film transfer gate 34-36 formation, contact to gate 35 and metal 38 formation, upper dielectric 28 formation and plug 39 formation. This module layer is fabricated using a series of predetermined processing steps. A first manufacturing embodiment is disclosed by Sugi on para 7, lines 3-49 with respect to Figs. 8 & 9 for a programmable interconnect structure. This embodiment clearly indicating that both via between 30 and 32 as well as thin-film transfer gate comprising elements 34-36 are both included in the manufacturing process. There is no analogous customized interconnect structure alternative for the second module. A second manufacturing embodiment with respect to Fig-14 is described in para 8, lines 19-44, also for a programmable interconnect structure. In the second embodiment, the thin-film transfer gate is constructed in a vertical dimension. This embodiment also indicates that via between wires 30 and 32 as well as thin-film transfer gate comprising elements 34-36 are both included in the manufacturing process of the second module layer. There is no analogous customized interconnect structure alternative for the second module. Every embodiment shown for manufacturing the second module by Sugi is to illustrate different embodiments of constructing programmable thin-film transfer gates above logic gates. There is no demonstration of a second module layer comprising a permanent interconnect structure

equivalent to a programmable interconnect structure in all of Sugi manufacturing embodiments.

In contrast, the Applicant illustrates the two selectable manufacturing configurations of connecting an array of first module layer structured cells in the two figures 7.6 & 7.7 of the application. Fig-7.6 shows the first selectable programmable manufacturing configuration. In that, three layers of metal are shown – bottom layer, second layer & top layer. The second module layer is defined from second metal definition, intermediate thin-film transistor formation steps, to the top metal definition. The top metal connects to the second metal through the programmable thin-film transistors in between. An ON transistor connects the two metal lines, while an OFF transistor disconnects the two metal lines. The ON/OFF data is held in a memory element. This ON/OFF connection is user programmable and further shown and described in Figs. 8A, 9A & 10A. The memory element holding the programmability may be also constructed in the very same thin-film layers. In Fig-7.7, the second selectable manufacturing configuration is shown. In that, an extra layer of metal, third layer, is inserted in between the top layer and the second layer of metal. Now the second module layer is defined from second metal definition, intermediate third metal definition, to the top metal definition. In this second module layer, the second metal definition and top metal definition (the first and last steps) has remained identical between the two manufacturing configurations: only the middle processing steps have altered between the two options. The new third layer of metal replaces the thin-film transistors shown in Fig-7.6. Module layer one did not change. Thus it is a second manufacturing configuration. Presence or absence of the third metal line makes or breaks the connection between the top metal and the second metal. This too is user programmable at the manufacturing stage: by duplicating the ON/OFF characteristic of the prior option thin-film transistor with appropriate metal connections. The metal connection options are further discussed with respect to Figs. 8B/8C, 9B/9C and 10D/10E. In the second configuration, the transistors sandwiched between the top and second metal are completely eliminated from the fabrication method.

As described herewith under Claim-11 rejection section, one with ordinary skill would not have the rationale to modify the Sugibayashi invention to construct two selectable manufacturing configurations for the second module layer to connect structured cells in the first module layer. Sugibayashi uses SRAM located in the first module layer to control the transfer gates in the second module layer. In Fig-14A, there has to be a control signal emanating from an SRAM cell coupled to the gate node 35/38 of the transfer-gate device with elements 34-36 (such

as the connection from cell 5a to Qe in Fig-5). The SRAM memory is in the first module layer and the transfer gate is in the second module layer. How the SRAM memory content and the TFT transistors could be replaced by customized interconnect structure in only the second module layer for a second manufacturing option is beyond the scope of Sugibayashi teaching. Hence a *prima facie* case of obviousness has not been met; it would not be obvious to one with ordinary skill to arrive at the Applicants claim stated in the independent claim 18. Applicants Claim-18 would have not been obvious under Sugibayashi, and withdrawal of the rejection of Claim-18, and those dependent thereupon (Claims 19-22) is respectfully requested.

Allowable subject matter:

Dependent Claim-23 objection: With respect to Applicant's claim 23, in the Office Action, section 20, the examiner noted that:

> "Claim 23 is objected as being dependent upon rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims."

The Applicant has herewith presented arguments as to why independent Claim-18 is distinctly different from Sugibayashi invention sighted in this office action. Withdrawal of that rejection was requested, and if granted, it would absolve the objection to Claim-23. Withdrawal of the objection by the examiner, in view of the requested withdrawal of Claim-18 rejection, is respectfully requested.

In summary, the Applicant submits that all claims as presented in this response are allowable in view of the Sugibayashi prior art sighted by the examiner, and withdrawal of all objections and rejections is respectfully requested.

CONCLUSION

The applicant believes that the above submission is fully responsive to the office action.

If for any reason the Examiner believes that a telephone conference would in any way expedite this matter, the Examiner is invited to telephone the Inventor Mr. Madurawe at (408) 737-8868 or on his cell phone at (408) 431-5367.

Respectfully submitted,

Raminda Madurawe

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